REMARKS/ARGUMENTS

This is Applicants' response to the Office Action of March 21, 2003, in which all the claims 1-20 in the case were rejected. Applicants respectfully request reconsideration in view of the above amendments, and the following arguments and remarks.

The Specification was objected to on the basis of informalities related to typographical errors. Claim 1 and Claim 11 have both been amended in a manner, which is believed to overcome the objection and withdrawal of the same is respectfully requested.

The drawings were objected to on the basis that the legend (Prior Art) was not designated with respect to Figures 1A-G. A new sheet of drawings have been submitted wherein Figures 1A-G have been properly designated with the legend (Prior Art).

The drawings were also objected to on the basis that the Figures did not conform to the Specification. Specifically, the Examiner has raised issues with respect to Figures 2E, 2F and 3B, which show a photoresist layer (40), but the Examiner has taken a position that the Specification indicates that the photoresist layer (40) has been removed. Applicants have submitted new sheets of drawings to correctly remove the photoresist layer (40) with respect to Figures 2E and 2F. However, Applicants maintain that Figure 3B is consistent with the Specification. The Examiner's attention is respectfully directed to page 17, lines 1-2 of the instant application, which states that the photoresist layer 40 is removed by etching as shown in

Figure 3C. Figure 3B, as filed, shows the photoresist layer present and Figure 3C, as filed, shows the photoresist layer 40 removed. Withdrawal of the objection with respect to Figures 2E, 2F and 3B is respectfully requested.

Claim 11 had been rejected under second paragraph of 35 USC 112 on the basis that the claim recites the limitation "after the hardbake step". Claim 11 has been amended in a manner, which is believed to provide adequate antecedent basis for the limitations now in the claim. Withdrawal of the rejection is respectfully requested.

Claims 1-20 had been rejected under 35 USC 103 as being unpatentable over U.S. Patent No. 6,179,200 to Kung, et. al. in view of U.S. Patent No. 5,251,806 to Agrwala, et. al. and further in view of non-patented publication Gilleo (Area Array Packing Handbook).

The Examiner has taken the position that "the claims recite methods of increasing the height of a solder bump by additional depositions of second and third metallurgies. Photolithographic, electro- and electroless-plating techniques are used. The claims further recite process steps and materials including sputter cleaning the pads, electro-plating conductive layers, electroless-plating the third layer and using solder, copper, nickel, gold and silver as plating materials". The Examiner has failed to establish a prima facie case of obviousness as required under 35 USC 103 because the Examiner has judged the "gist" of Applicants' invention. It is basic error for the Examiner to judge the "gist" or "idea" of the invention. As set forth in Jones v. Hardy, 727 F.2d 1524, 220 USPQ 1021 (Fed. Cir. 1984) the Federal Circuit stated that:

> The invention cannot be tested on the basis of whether the "idea" of using molded polystyrene is patentable. Under the patent statute, Title 35 USC "ideas" are not patentable, claims, structures and methods are. Reducing a claimed invention to an "idea," and then determining the patentability of that "idea" is error. (Citations omitted). Analysis properly begins with the claims for they measure and define the invention.

The Examiner's rejection of the claims fails to specifically address the limitations of Applicants' claims, specifically the specific sequence of acts called for in the claims, the specific materials used and the results achieved.

Kung, et. al. '200 patent teaches the method of forming solder balls that have improved height on electronic substrate, such as a silicon wafer. After solder bumps are deposited by a conventional method, such as evaporation, electro-plating, electroless-plating, or solder paste screen printing, the solder bumps are reflown on the substrate in an upside down position, such that gravity pulls down the solder ball and, thereby, increases its height. Kung, et. al. does not specifically teach using a flux agent on one layer of an electrically conductive material followed by deposing another layer of an electrically conductive material. Furthermore, none of the references relied on by the Examiner, including Gilleo disclose a relationship between the use of a flux agent and the manufacturing of tall bumps utilizing a series of deposited metal layers. Gilleo teaches the use of solder flux for attaching solder balls to another substrate, such as attaching the solder balls of a flip chip to a printed circuit board. There is no relationship or connection disclosed in the prior art between the use of a flux agent and making tall electrically conducted bumps. The mere fact that the use of solder flux or flux agent is known to those skilled in the art does not render Applicants claimed invention obvious. There are millions of

process steps and process materials known to those skilled in the art. There must be a suggestion in the prior art motivating a person of ordinary skill to choose one out of the millions of possible process steps or materials and in a specific sequence to arrive at Applicants claimed invention in order for applicant to be precluded from obtaining a patent under 35 USC 103. When there is no relationship suggested to exist in the prior art between a material and a result achieved by the claimed invention using the material in a specific way, the invention cannot be obvious under 35 USC 103. In re Herschler, 591 F.2d 693, 200 USPQ 711 (CCPA 1979).

Furthermore, Agarwala teaches the use of a capping material between multiple layers of solder to increase the height of a bump. Both Claim 1 and Claim 11 call for a third electrically conductive material deposited on the second electrically conducted material. Agarwala, et. al. teaches depositing a third solder layer 36 on a cap layer 29, which is over the second solder layer 26. As such, Agarwala, et. al. teaches away from Applicants claimed invention. Furthermore, the Examiner is taking the position that although the references do not teach hardbaking the photoresist, such a step is known to those skilled in the art. Again, the Examiner has not pointed to any disclosure establishing a relationship between hardbaking the photoresist and building tall bumps. Applicants' hardbaking results in a more uniform height of the bump on the wafer. See instant application at page 16 paragraph 44. Since there is no disclosed relationship between the hardbaking of the photoresist act and the making of tall bumps, the Examiner's mere statement that such a step is known in the prior art does not render the Applicants' claimed invention obvious under 35 USC 103. The rejection of Claims 1-20 in view of Kung, et. al. and Agarwala, et. al. and Gallieo is improper and withdrawal of the same is respectfully requested.

Claims 1 and 11 had been rejected under 35 USC 103 as being unpatentable over U.S. Patent No. 6,426,281 to Lin, et. al. in view of U.S. Patent No. 6,204,557 to Yanagida and further in view of U.S. Patent No. 6,426,176 to Danielson, et. al. and further in view of U.S. Patent No. 6,440,836 to Lu and further in view of U.S. Patent No. 6,391,023 to Stuby. Applicants maintain that the Examiner has failed to establish a prima facie case of obviousness under the rejection.

Lu '281 discloses depositing layers 46 and 48 of respectively cooper and titanium over and under bump metallurgy layer. The layers 46 (copper) and 48 (titanium) are plated over the under bump metallurgy using conventional electro-plating. See column 9, lines 57-56. A layer 50 of solder is deposited over layer 48. Lu, et. al. fails to disclose applying a fluxing agent to a layer of electrically conductive material prior to depositing a subsequent layer of electrically-conductive material as called for in Applicants' Claims 1 and 2. Again, no connection or relationship is disclosed in the prior art with respect to the use of a flux agent to build bumps of improved height or tall bumps.

Yanagida '558 discloses forming a bump, including a relatively elastic first ball bump formed on an electrode pad provided on a semi-conducted devise, on a second ball bump formed in such a manner as to overlap on the first ball bump at least in the direction perpendicular to the electrode pad. The second ball bump is different in material or composition from the first ball bump and is adapted to be in contact with and eutectic solder pre-coated on a conventional land of a circuit board. After the first solder ball bump is deposited, it is firmly held by a resin layer 21. The first ball bump may be planarized and a second ball bump deposited thereon. Again,

Yanagida '558 fails to disclose the use of a flux agent on a first or second electrically conductive layer prior to depositing a subsequent electrically conductive layer as called for in Applicants' Claims 1 and 11.

Danielson, et. al. '176 is directed to solving a problem related to corrosion of lead-based bumps (such as solder bumps) that produce a high contact resistance that may result in a chemical tester not accurately testing the speed or functionality of an integrated circuit using such bumps. See column 1, lines 38-48. To solve the problem, Danielson, et. al. deposits a protective layer 124 or 224 over the lead-based bump. Danielson, et. al. is not directed to producing bumps of improved height or tall bumps. Again, Danielson, et. al., like the other references relied on by the Examiner, fails to disclose any connection or relationship to the use of a flux agent applied to a first or second electrically-conductive layer in a bump stack followed by the subsequent depositing of another electrically-conductive layer.

Stuby fails to overcome the deficiencies of the other references relied on in the rejection.

The rejection fails to even address the use of a flux agent. Again, Applicants respectfully submit that the Examiner has rejected the "gist" or "idea" of Applicants' invention, which is clear error and improper under 35 USC 103.

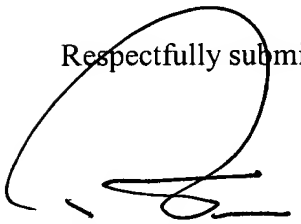
Applicants have added new claims calling for a method including electroplating a second layer on a first layer of electrically conductive material while a photoresist layer is still on the

semiconductor device. None of the references of record suggest such a method. Notice of allowance of the new claims is respectfully requested.

Please charge deposit account number 50-0484 for the fee associated with adding the new claimS.

In view of the above amendments and remarks, applicants respectively request reconsideration and allowance of all the claims now in the case.

Respectfully submitted



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